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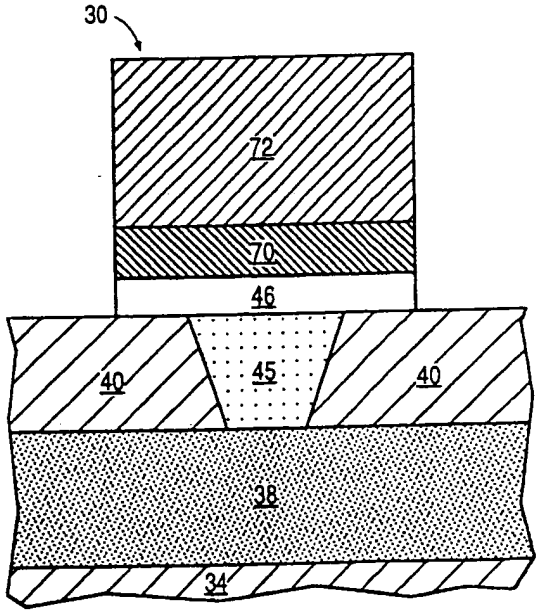


(57) Abstract

An amorphous silicon antifuse (30) is formed between two electrodes. The bottom electrode (45) is a plug, of tungsten in one embodiment, formed in a via in a dielectric layer (40). The top surface of the plug is coplanar with the top surface of the dielectric layer. Thus the amorphous silicon layer above the plug is planar, as is the top electrode layer above the amorphous silicon. Deposition of the amorphous silicon (46) and of the top electrode is facilitated thereby. The electrical characteristics of the antifuse are tightly controlled. The antifuse has a simple structure, a small size, small capacitance in the unprogrammed condition, and small leakage current. The antifuse can be made with relatively few process steps. The process sequence provides a planar top surface for the amorphous silicon deposition and the top electrode (70, 72) formation.

AMORPHOUS SILICON ANTIFUSES AND METHODS FOR FABRICATION THEREOF

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to programmable integrated circuit structures and methods for fabrication thereof, and more particularly to amorphous silicon antifuses and circuits and routing structures incorporating antifuses, and methods for fabrication thereof.

Description of Related Art

Programmable semiconductor devices include programmable read only memories ("PROMs"), programmable logic devices ("PLDs"), and programmable gate arrays. Programmable elements suitable for one or more of these device types include fuses and antifuses.

A fuse is a structure which electrically couples a first terminal to a second terminal, but which, when programmed by passage of sufficient current between its terminals, electronically decouples the first terminal from the second terminal. A fuse typically is of a conductive material which has a geometry that causes portions of the conductive fuse material to physically separate from each other when heated to the extent that an open circuit results.

An antifuse is a structure which when unprogrammed does not electrically couple its first and second terminals, but which, when programmed by applying sufficient voltage between the first and second terminals, permanently electrically connects the first and second terminals. One type of antifuse comprises an amorphous silicon which forms conductive polysilicon when heated.

15, which fully overlays and contacts the barrier metal 11 under the via. Second metal comprising barrier metal 16 and aluminum conductor 17 is provided over the via, in contact with the amorphous silicon 15.

The contact antifuse of Figure 2 is formed over a transistor comprising collector 20, base 21, and emitter 22. Emitter contact is made to a platinum silicide region 23 through a contact hole in oxide 24, which is lined with amorphous silicon film 25. Barrier metal 26 and aluminum conductor 27 overlay the amorphous silicon 25, and are protected by oxide 28.

In the examples of Figures 1 and 2, the deposition of the amorphous silicon was a critical step in the process, as the thickness of the film 15 (Figure 1) and film 25 (Figure 2) was thought to control the programming voltage. The pre-programmed leakage current was reduced to about 6 microamperes at 2 volts by a high temperature anneal at 450 degrees C. Other factors thought to influence leakage current in the undoped amorphous silicon antifuse were feature size (leakage current proportional) and film thickness (leakage current inversely proportional).

Unfortunately, antifuse technology developed for use in memories is generally too leaky for use in PLDs, as noted by Cook et al. In a PROM, one bit is selected per output at a time; therefore, if the programmable elements are leaky, only one leaky bit loads the sense amplifier. Usually the sense amplifier can tolerate this loading without drastically affecting its functionality or performance. Contrast one type of PLD known as a programmable array logic, which is implemented using PROM technology. The programmable elements are used to configure logic (routing is dedicated and global). In programmable array logic, multiple bits can be accessed and may overload the sense line if the programmable elements are leaky. Overloading the sense line may drastically degrade the performance and in the extreme case, may result in functional failure.

SUMMARY OF THE INVENTION

Some embodiments of the amorphous silicon antifuses of the present invention have a simple structure, a small size, small capacitance in the unprogrammed condition, small leakage current, and highly reproducible and controllable physical and electrical characteristics. Their manufacture requires very few process steps, and the process sequence provides a planar top surface for almost all the steps. In particular, the amorphous silicon is planar in some embodiments so that a high quality, uniform thickness deposition thereof is facilitated. The electrode overlaying the amorphous silicon is also planar in some embodiments, and the electrode fabrication is thereby facilitated.

These and other advantages are achieved in some embodiments of the antifuse structure according to the present invention. The structure generally includes a dielectric layer having an opening therethrough; a conductive plug filling the opening, a top surface of the plug being substantially coplanar with a top surface of the dielectric layer; an amorphous silicon layer overlaying and contacting the plug; and a conductor overlaying and contacting the amorphous silicon layer.

Further, a method is provided for fabricating an antifuse structure. The method generally includes the steps of fabricating an insulating layer; fabricating an opening through the insulating layer at a selected location; fabricating a plug of conductive material in the opening so that a top surface of the plug is substantially coplanar with a top surface of the insulating layer; fabricating a layer of amorphous silicon overlaying and contacting the plug; and fabricating a conductor overlaying and contacting the amorphous silicon layer.

The invention further provides a programmable interconnect structure, a field programmable gate array, and a method for fabricating a field programmable gate array.

a thin layer of titanium covered by a thicker layer of aluminum. Other conductive layers are suitable as well.

A second dielectric layer 40 is formed on the first conductive layer 38. The second dielectric layer 40 is patterned to form vias, such as via 44, exposing the first conductive layer 38. Some of these vias, in particular via 44, will serve as sites for antifuses. Other vias, not shown, may allow for direct connection between first conductive layer 38 and a to-be-formed second conductive layer.

As shown in Figure 4, a plug 45 of conductive material is formed in via 44 so as to fill the via. Plug 45 provides the bottom electrode of the antifuse. The top surface of the plug 45 is substantially coplanar with the top surface of the second dielectric layer 40. Consequently, a to-be-formed amorphous silicon layer 46 (Figure 6) will be planar. Formation of high quality, uniform layer 46 is thereby facilitated.

In one embodiment, the plug 45 is made of tungsten. Tungsten plugs have been used to provide interlevel contacts between different conductive layers. Any suitable tungsten plug deposition technique may be used. For example, in one technique, the plug 45 is formed by selective chemical vapor deposition ("CVD") of tungsten in the via 44. At the bottom of via 44, the material of first conductive layer 38 reacts with gaseous reactants so as to form tungsten in via 44. No tungsten is deposited, however, on top of the second dielectric layer 40 during the selective CVD. Selective CVD of tungsten is described generally in R.V. Joshi et al., "Low-Resistance Submicron CVD W Interlevel Via Plugs on Al-Cu-Si," VMIC Conference, June 12-13, 1989, pp. 113-121, available from the Institute of Electrical and Electronic Engineers ("IEEE") of Piscataway, New Jersey and hereby incorporated herein by reference thereto. See also T. Ohba, "Selective and Blanket Tungsten Interconnection and its Suitability for 0.2-Micron ULSI," VMIC Conference, June 12-13, 1990,

disclosure is hereby incorporated herein by reference thereto, the thickness of amorphous silicon layer 46 in contact with the plug 45 is an important factor in controlling the programming voltage and leakage current of the antifuse. In this embodiment, the thickness of amorphous silicon layer 46 is about 1,600 angstroms. Of course, other thicknesses are suitable depending on the programming voltage desired.

As described in the above-mentioned application Serial No. 07/447,969, another factor controlling leakage current is the manner of deposition of the amorphous silicon layer 46. In one embodiment, the amorphous silicon layer 46 is deposited using plasma enhanced chemical vapor deposition ("PECVD"). A suitable reactor is the Concept One reactor available from the Novellus Systems, Inc., San Jose, California. Suitable reactants and process parameters are described generally in the above-mentioned application Serial No. 07/447,969.

As shown in Figure 6, the second electrode of the antifuse 30 is formed by sputter depositing an about 2,000 angstrom layer 70 of titanium tungsten (TiW) and an about 8000 angstrom layer 72 of aluminum-copper (AlCu). TiW layer 70 and AlCu layer 72 are patterned to form the second electrode. The mask used for patterning the second electrode layers 70 and 72 is smaller than the mask used to pattern the amorphous silicon 46 so that, in the worst misalignment case, the entire second electrode is above amorphous silicon 46. Portions of the amorphous silicon 46 that are exposed by the second electrode mask are etched away when layers 70 and 72 are etched during the second electrode formation.

Layers 70 and 72 are planar above the amorphous silicon layer 46. The planarity facilitates deposition of layers 70 and 72. TiW layer 70 is a barrier layer that serves to prevent the aluminum of AlCu layer 72 from spiking into the amorphous silicon 46. Aluminum spikes would increase the leakage current or might even cause a

Arsenide, and others.

Substrate 100 is provided with a P-doped substrate region 104. An NMOS device 162 that forms part of logic or I/O circuits of the gate array comprises source and drain regions 112 and 114 and gate 116. Patterned oxide layers 118, 119 and 120 (shown in cross hatch) also are present. As is well known in the art, oxide layer 118 is a field oxide, boro-phosphosilicate glass layer 119 is a contact oxide, and oxide layer 120 comprises various oxide layers (not shown) formed in the fabrication of gate 116. The oxide layers 118, 119 and 120 are suitably patterned and etched to form contact holes down to the various source and drain regions including regions 112 and 114.

Using standard techniques, a film of aluminum measuring about 6,000 angstroms is sputtered over the patterned oxide layers and into the contact holes to regions 112 and 114. Other metals may be used as well. Aluminum film 38 corresponds to the first conductive layer 38 of Figures 3-6. First metal lines are formed by patterning and etching aluminum film 38 using a BCl_3, Cl_2, $CHCl_3$ standard aluminum dry etch.

The intermetal dielectric is a thick oxide layer 40 of about 9,000 angstroms thickness, deposited using any suitable standard technique such as, for example, plasma enhanced chemical vapor deposition. Layer 40 corresponds to the second dielectric layer 40 of Figures 3-6. In one of many suitable techniques, the layer 40 comprises two oxide layers (not shown). The first oxide layer is deposited to the selected thickness and planarized. The planarization step involves spinning a resist layer over the deposited oxide and reflowing the resist with a postbake, after which the surface is planarized in an RIE etch-back adjusted for equal resist and oxide etch rates. A second oxide layer then is deposited to ensure dielectric integrity and the 9,000 angstrom thickness over the irregular topography.

Antifuse vias 44a and 44b are now formed through the

The second level routing channels extend generally orthogonally to the first level routing channels in a conventional layout shown, for example, in U.S. Patent No. 4,914,055, issued April 3, 1990 to Gordon et al., the disclosure of which patent is hereby incorporated herein by reference thereto. The thick oxide 40 serves to reduce the capacitance between the first level routing channels and the second level routing channels. In spite of the large thickness of oxide layer 40, vias 44 can be made narrow because good quality plugs 45 providing a good contact to aluminum layer 38 can be formed even in narrow vias. Significant size reduction of the gate array is thereby made possible. Leakage current and the capacitance of the unprogrammed antifuse are also reduced thereby.

While the invention has been described with respect to the embodiments included above, other embodiments and variations not described herein may be considered to be within the scope of the invention. For example, the invention should not be limited by the composition of the metal system used for the interconnects, or to any specific thickness of the various films and oxides used in the structure. These other embodiments and variations are to be considered within the scope of the invention, as defined by the following claims.

7. An antifuse structure as in Claim 6 wherein said portion is substantially planar and wherein said portion extends at least over the entire top surface of said plug.

8. An antifuse structure as in Claim 1 wherein said plug completely fills said opening.

9. An antifuse structure as in Claim 1 wherein said plug comprises tungsten.

10. An antifuse structure as in Claim 28 wherein said amorphous silicon is about 1,600 angstroms thick.

11. An antifuse structure as in Claim 1 wherein said dielectric layer is about 9,000 angstroms thick.

12. An antifuse structure as in Claim 28 wherein said conductor comprises:

a layer of TiW; and

a layer of aluminum separated from said programmable material layer by said layer of TiW.

13. A method for fabricating an antifuse structure, comprising the steps of:

fabricating an insulating layer;

fabricating an opening through said insulating layer at a selected location;

fabricating a plug of conductive material in said opening so that a top surface of said plug is substantially coplanar with a top surface of said insulating layer;

fabricating a layer of amorphous silicon overlaying and contacting said plug; and

fabricating a conductor overlaying and contacting said amorphous silicon layer.

14. A method as in Claim 13 wherein said conductive

said step of depositing a layer of aluminum comprises the step of depositing aluminum using sputtering.

22. A programmable integrated circuit comprising:

a semiconductor structure having circuit elements in a substrate;

a first level of conductive routing channels, said first level channels being connected to selected circuit elements;

an insulating layer overlaying said first level routing channels, said insulating layer having openings formed therein at selected locations;

a conductive plug in each of said openings, each plug contacting said first level routing channels, a top surface of said insulating layer having, for each plug, a portion adjacent the respective plug, each portion being substantially coplanar with a top surface of the respective plug;

a layer of programmable material overlaying and contacting said plugs, said programmable material being non-conductive when said integrated circuit is unprogrammed, said programmable material providing one or more conductive paths therethrough when said integrated circuit is programmed, said programmable material layer having, for each plug, a substantially planar portion which overlays the plug and also overlays the respective adjacent portion of the top surface of said insulating layer; and

a second level of conductive routing channels, said second level channels being connected to selected circuit elements, said second level channels overlaying and contacting said programmable material layer at said selected locations.

23. A programmable integrated circuit as in Claim 22, wherein said openings terminate at said first level

27. A method as in Claim 26 wherein said second level channels are substantially orthogonal to said first level channels.

28. An antifuse structure as in Claim 1 wherein said programmable material comprises amorphous silicon.

29. An antifuse structure as in Claim 1 wherein said conductor comprises:

a layer of conductive material; and

a barrier layer separating said conductive material from said programmable material for preventing the conductive material from spiking into said programmable material.

30. A programmable integrated circuit as in Claim 22 wherein said programmable material comprises amorphous silicon.

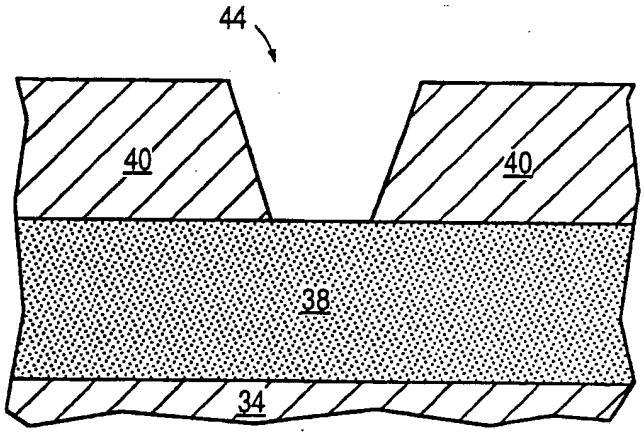


FIG. 3

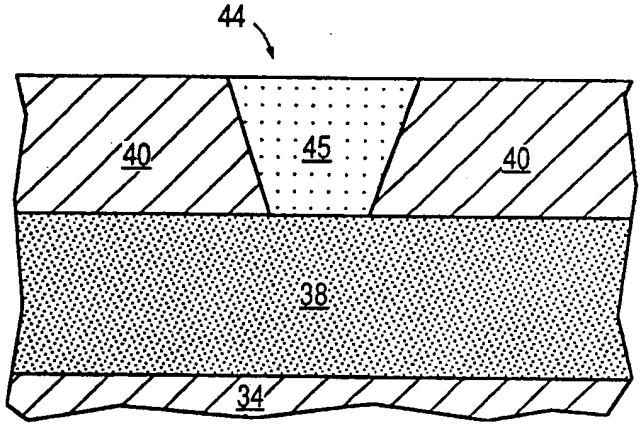
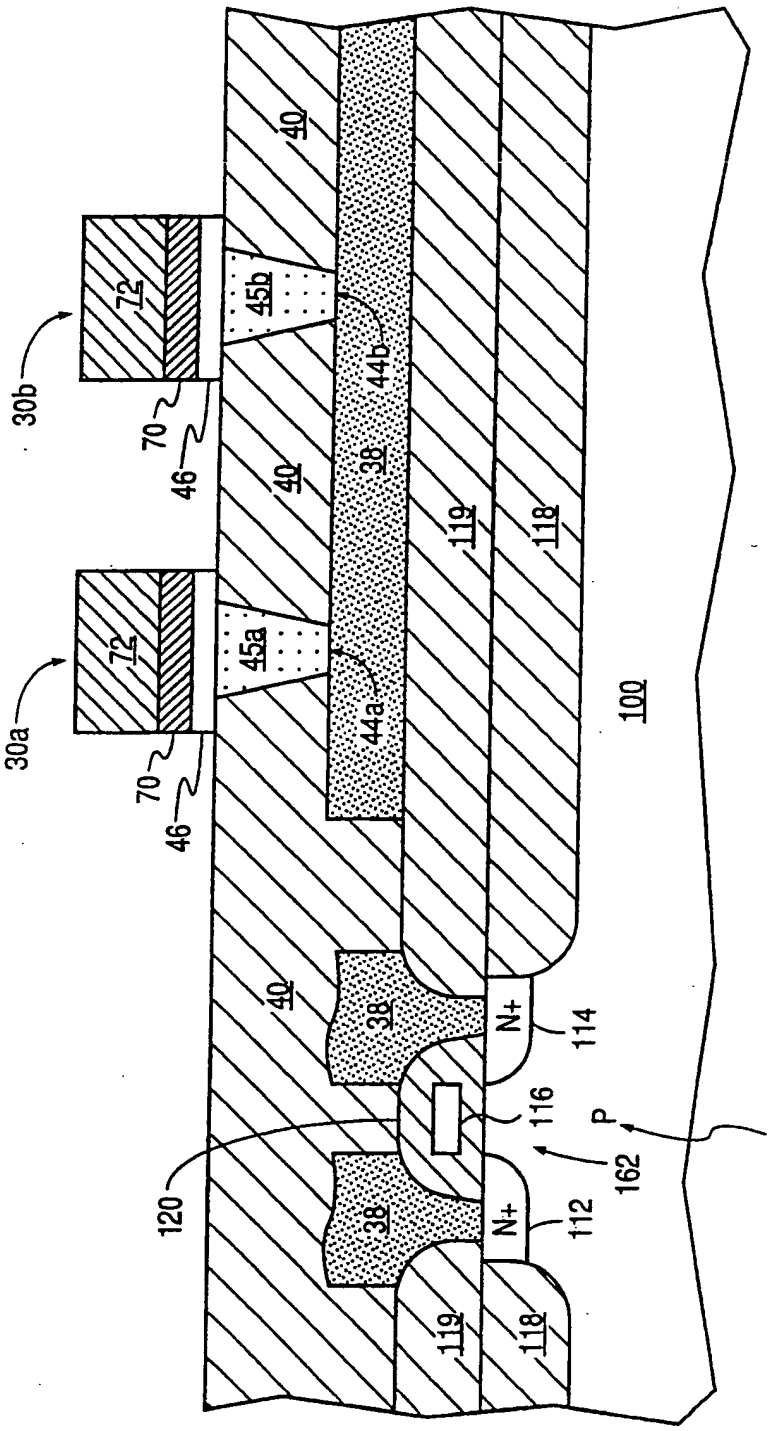


FIG. 4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116
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162
120
38
N+
112
119
118
100

FIG. 7